In re Appln. of Yuushin YAMAMOTO
Application No. Unassigned

CLAIM AMENDMENTS

1. (Currently Amended) A system for operating in parallel a plurality of non-break power units inserted separately between (i) a bypass power source and a plurality of input power sources ~~on one hand~~ and (ii) a parallel bus ~~on the other hand~~,

each of said non-break power units comprising:

an inverter inserted between ~~said~~ an input power source and ~~said~~ the parallel bus; and

an AC switch inserted between ~~said~~ the bypass power source and ~~said~~ the parallel bus;

each of said non-break power units having:

an inverter power supply mode in which power ~~supply is performed~~ is supplied from ~~said~~ the input power source to ~~said~~ the parallel bus by way of said inverter with said AC switch ~~being opened~~ open; and

a bypass power supply mode in which, when operation of said inverter stops, said AC switch is closed to ~~thereby~~ enable the AC power to be supplied ~~straightforwardly~~ directly to said parallel bus from said bypass power source by way of said AC switch,

~~wherein~~ each of said non-break power units further ~~comprises~~ comprising.

a sequence control circuit for generating an output signal corresponding to an inverter power supply signal;

a switching element for outputting ~~said~~ the inverter power supply signal based on ~~the basis of~~ the output signal of said sequence control circuit; and

a switch driving circuit for generating a driving signal for said AC switch in response to ~~said~~ the inverter power supply signal, wherein

output terminals of said switching elements incorporated in said plurality of non-break power units, respectively, are connected in parallel with one another, and

~~wherein~~ said switch driving circuit incorporated in each of said non-break power units ~~is so designed as to generate~~ generates the driving signal ~~to~~ for the associated AC switch based on ~~the basis of~~ a composite signal generated by synthesizing the inverter power supply signals in said ~~individual~~ non-break power units.

2. (Currently Amended) ~~A~~ The non-break power unit parallel operating system according to claim 1, wherein the output terminals of said switching elements incorporated in

said ~~individual~~ non-break power units are connected in parallel with one another in a loop-like form.

3. (Currently Amended) ~~A~~ The non-break power unit parallel operating system according to claim 1, wherein each of said non-break power units further comprises:

a switch inserted on ~~the~~ an output side of said non-break power unit, and

an auxiliary contact of said switch inserted on ~~the~~ an input terminal side of said switching element of said non-break power unit, ~~wherein~~ and said switching element ~~is so designed as to output said~~ outputs the inverter power supply signal by additionally taking into account a state signal of said switch of ~~the~~ said non-break power unit to which said switching element belongs, as a condition for enabling ~~said~~ the inverter power supply signal to be ~~outputted~~ output.

4. (Currently Amended) ~~A~~ The non-break power unit parallel operating system according to claim 3, wherein said switch driving circuit of each of said non-break power units ~~is so designed as to output~~ outputs a driving signal for said AC switch by additionally taking into account the state signal of ~~the~~ said switch of ~~the~~ said non-break power unit to which said switch driving circuit belongs, as a condition for enabling ~~said~~ the driving signal to be ~~outputted~~ output.

5. (Currently Amended) ~~A~~ The non-break power unit parallel operating system according to claim 1, wherein

each of said non-break power units further comprises an inverter power supply state detecting circuit inserted between the output terminal of said switching element and said switch driving circuit,

said inverter power supply state detecting circuit ~~being comprised of~~ comprises:

a photo-coupler connected to the output terminal of said switching element, and

a diode connected in series to said photo-coupler, wherein the composite signal derived from ~~synthesization of~~ synthesizing the inverter power supply signals is detected by said photo-coupler and said diode.

6. (Currently Amended) ~~A~~ The non-break power unit parallel operating system according to claim 1, wherein

each of said non-break power units further ~~comprising~~ comprises a synchronous/asynchronous state detecting circuit for detecting ~~a~~ synchronous/asynchronous state between the output voltage of said inverter and that of said bypass power source to ~~thereby~~ output a synchronous state signal, ~~wherein~~ and

said switch driving circuit ~~is so designed as to output~~ outputs a driving signal for said AC switch by additionally taking into account the synchronous state signal in ~~the~~ said non-break power unit to which said switch driving circuit belongs, as a condition for enabling ~~said~~ the driving signal to be ~~outputted~~ output.

7. (Currently Amended) ~~A~~ The non-break power unit parallel operating system according to claim 6, ~~said~~ wherein

the synchronous state signal containing an asynchronism signal ~~indicating~~ indicates an asynchronous state between the output voltage of said inverter and the voltage of said bypass power source, ~~wherein the~~ and

an output terminal ~~of said~~ for the asynchronism signal is connected in parallel to the output terminal for the asynchronism signal of the other non-break power unit.

8. (Currently Amended) ~~A~~ The non-break power unit parallel operating system according to claim 6, ~~said~~ wherein

the synchronous state signal ~~containing~~ contains a synchronism signal indicating a synchronous state between the output voltage of said inverter and the voltage of said bypass power source, ~~wherein the~~ and

an output terminal ~~of said~~ for the synchronism signal is connected in parallel to the output terminal for the synchronism signal of the other non-break power unit.

9. (Currently Amended) ~~A~~ The non-break power unit parallel operating system according to claim 6, wherein each of said non break power units further ~~comprising~~ comprises:

a delay circuit for delaying the output signal of said sequence control circuit for a predetermined time;

an AND circuit for determining a logical product of ~~said~~ the synchronous state signal and the output signal of said delay circuit: and

an OR circuit for determining a logical sum of the output signal of said AND circuit and the output signal of said sequence control circuit, wherein a logical sum signal ~~outputted~~ output from said OR circuit is ~~inputted~~ input to said switching element.